Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OSC IN**
2. **OSC OUT**
3. **OEH**
4. **GND / OSCLO 1 (2 bond pads)**
5. **OUT**
6. **VCC**
7. **OSC DR**
8. **DIVB**

**MASK**

**REF**

**2**

**1**

**4**

**4**

**5**

**6**

**.062”**

**7 8**

**3**

**.062”**

**J33Ø1Z**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref: J33Ø1Z**

**APPROVED BY: DK DIE SIZE .062” X .062” DATE: 7/31/23**

**MFG: FAIRCHILD THICKNESS .015” P/N: 74ACT3301**

**DG 10.1.2**

#### Rev B, 7/19/02